WHAT IS CLAIMED:

1. A flash memory comprising:

a first redundancy circuit configured to provide read repair information for read operations to the flash memory; and

a second redundancy circuit, separate from the first redundancy circuit, configured to provide write repair information for write operations to the flash memory.

2. A flash memory according to Claim 1 wherein the read repair information and the write repair information are associated with a same address of a defective memory cell in a bank of the flash memory.

3. A flash memory according to Claim 2:

wherein the first redundancy circuit does not provide the read repair information for write operations to the bank; and

wherein the second redundancy circuit does not provide the write repair information for read operations to the bank.

4. A flash memory according to Claim 2 wherein the bank comprises a first bank of the flash memory:

wherein a first entry in the first redundancy circuit includes an address of a first defective memory cell in the bank associated with the read repair information; and

wherein a second entry in the first redundancy circuit includes an address of a second defective memory cell in a second bank of the flash memory that is separate from the first bank.

5. A flash memory according to Claim 1 wherein the flash memory is configured to perform a first read or write operation in a first sector of a bank of the flash memory while simultaneously performing a second read or write operation in a second sector of another bank of the flash memory.

6. A flash memory according to Claim 1 wherein the first redundancy circuit is dedicated to storing addresses of defective memory cells and associated read repair information provided for read operations in any of a plurality of banks of the flash memory; and

wherein the second redundancy circuit is dedicated to storing the addresses of the defective memory cells and associated write repair information for write operations in any of the plurality of banks of the flash memory.

7. A flash memory device according to Claim 1 wherein the flash memory comprises a NOR or NAND type flash memory.

8. A flash memory according to Claim 1 wherein the read repair information and the write repair information comprise identical information.

9. A flash memory comprising:

a first redundancy circuit configured to store an address of a defective memory cell in the flash memory; and

a second redundancy circuit, separate from the first redundancy circuit, configured to store the address of the defective memory cell.

10. A flash memory according to Claim 9 wherein the first redundancy circuit is configured to provide read repair information for a read operation to the flash memory and the second redundancy circuit is configured to provide write repair information for a write operation to the flash memory.

11. A flash memory according to Claim 10:

wherein the first redundancy circuit is configured to not provide the read repair information for the write operation; and

wherein the second redundancy circuit is configured to not provide the write repair information for the read operation.

12. A flash memory according to Claim 10 further comprising:

a plurality of banks of the flash memory, wherein the first redundancy circuit is configured to provide the read repair information for the read operation to any of the plurality of banks; and

wherein the second redundancy circuit is configured to provide the write repair information for the write operation to any of the plurality of banks.

13. A flash memory according to Claim 9:

wherein the first redundancy circuit provides read repair information for the read operation indicating at least one defective bit position at the address to be read; and

wherein the second redundancy circuit provides write repair information for the write operation indicating at least one defective bit position at the address to be written.

14. A flash memory according to Claim 13 further comprising:

a sense amplifier circuit electrically coupled to first redundancy circuit wherein the read repair information is provided to the sense amplifier circuit during the read operation via read repair lines; and

a write driver circuit electrically coupled to the second redundancy circuit wherein the write repair information is provided to the write driver circuit during the write operation via write repair lines that are separate from the read repair lines.

15. A flash memory according to Claim 13 wherein a read address is provided to the first redundancy circuit via read address lines during the read operation and a write address is provided to the second redundancy circuit during the write operation via write address lines that are separate from the read address lines.

16. A flash memory device according to Claim 9 wherein the flash memory comprises a NOR or NAND type flash memory.

17. A flash memory according to Claim 9 wherein the flash memory is configured to perform a first read or write operation in a first sector of a bank of the flash memory while simultaneously performing a second read or write operation in a second sector of another bank of the flash memory.

18. An integrated circuit memory device comprising:

a first redundancy circuit configured to store an address of a defective memory cell in the memory device; and

a second redundancy circuit configured to store the address of the defective memory cell.

19. An integrated circuit memory device according to Claim 18 wherein the address stored in the first redundancy circuit is accessed for a read operation to the defective memory cell in the memory and is not accessed for write operation to the defective memory cell.

20. An integrated circuit memory device according to Claim 19:

wherein the first redundancy circuit does not provide the address stored therein for a write operation to the memory cell; and

wherein the second redundancy circuit does not provide the address stored therein for a read operation to the memory cell.

21. An integrated circuit memory device according to Claim 18 wherein the memory cell is included in a first bank of the integrated circuit memory:

wherein a first entry in the first redundancy circuit includes an address of a first defective memory cell in the first bank; and

wherein a second entry in the first redundancy circuit includes an address of a second defective memory cell in a second bank of the flash memory that is separate from the first bank.

22. An integrated circuit memory device according to Claim 18 wherein the integrated circuit memory device is configured to perform a first read or write operation in a first sector of a bank of the memory while simultaneously performing a second read or write operation in a second sector of another bank of the memory.

23. An integrated circuit memory device according to Claim 18 wherein the first redundancy circuit is dedicated to storing addresses of defective memory cells and associated read repair information provided for read operations in any of a plurality of banks of the flash memory; and

wherein the second redundancy circuit is dedicated to storing addresses of defective memory cells and associated write repair information provided for write operations in any of the plurality of banks of the flash memory.

24. An integrated circuit memory device according to Claim 18 wherein the memory comprises a NOR or NAND type flash memory.

25. A flash memory comprising:

a dedicated-read operation redundancy circuit configured to provide read repair information; and

a dedicated-write operation redundancy circuit configured to provide write repair information.

26. A flash memory according to Claim 25:

wherein the dedicated-read operation redundancy circuit does not provide the read repair information in response to a write operation to a defective memory cell in the flash memory; and

wherein the dedicated-write operation redundancy circuit does not provide the write repair information in response to a read operation to the defective memory cell.

27. A flash memory according to Claim 25:

wherein a first entry in the dedicated-read operation redundancy circuit includes an address of a first defective memory cell in a first bank of the flash memory; and

wherein a second entry in the dedicated-read operation redundancy circuit includes an address of a second defective memory cell in a second bank of the flash memory that is separate from the first bank.

28. A flash memory according to Claim 25 wherein the flash memory is configured to perform a first read or write operation in a first sector of a bank of the flash memory while simultaneously performing a second read or write operation in a second sector of another bank of the flash memory.

29. A flash memory according to Claim 25 wherein the dedicated-read operation redundancy circuit is configured to store addresses of defective memory cells and the associated read repair information provided for read operations to defective memory cells in any of a plurality of banks of the flash memory; and

wherein the dedicated-write operation redundancy circuit is configured to store the addresses of the defective memory cells and the associated write repair information provided for write operations to the defective memory cells in any of the plurality of banks of the flash memory.

30. A flash memory device according to Claim 25 wherein the flash memory comprises a NOR or NAND type flash memory.

31. A flash memory comprising:

means for providing read repair information for read operations to the flash memory; and

means for providing write repair information, separate from the means for providing the read repair information, for write operations to the flash memory.

32. A flash memory according to Claim 31 wherein the read repair information and the write repair information are associated with a same address in a bank of the flash memory.

33. A flash memory according to Claim 32:

wherein the means for providing the read repair information does not provide the read repair information for write operations to the bank; and

wherein the means for providing write repair information does not provide the write repair information for read operations to the bank.

34. A flash memory according to Claim 32 wherein the bank comprises a first bank of the flash memory:

wherein a first entry in the means for providing read repair information is associated with an address of a first defective memory cell in the bank; and

wherein a second entry in the means for providing read repair information is associated with an address of a second defective memory cell in a second bank of the flash memory that is separate from the first bank.

35. A flash memory according to Claim 31 wherein the flash memory is configured to perform a first read or write operation in a first sector of a bank of the flash memory while simultaneously performing a second read or write operation in a second sector of another bank of the flash memory.

36. A flash memory according to Claim 31 wherein the means for providing read repair information is dedicated to storing addresses of defective memory cells and associated read repair information provided for read operations in any of a plurality of banks of the flash memory to repair defects in read data due to the defective memory cell; and

wherein the means for providing write repair information is dedicated to storing the addresses of the defective memory cells and associated write repair information for write operations in any of the plurality of banks of the flash memory to avoid writing data to the defective memory cell.

37. A flash memory device according to Claim 31 wherein the flash memory comprises a NOR or NAND type flash memory.

38. A method of operating a flash memory device comprising:

storing read repair information associated with a first defective memory cell in a first redundancy circuit;

storing write repair information associated with a second defective memory cell in a second redundancy circuit that is separate from the first redundancy circuit;

providing the read repair information from the first redundancy circuit for read operations to the memory cell to repair data read from the first defective memory cell; and

providing the write repair information from the second redundancy circuit for write operations to the memory cell to avoid writing data to the second defective memory cell.

39. A method according to Claim 38 wherein the flash memory is configured to perform a first read or write operation in a first sector of a bank of the flash memory while simultaneously performing a second read or write operation in a second sector of another bank of the flash memory.

40. A method according to Claim 39, wherein the first redundancy circuit is configured to not provide the read repair information for the write operation; and

wherein the second redundancy circuit is configured to not provide the write repair information for the read operation.

41. A method according to Claim 40, further comprising:

a plurality of banks of the flash memory, wherein the first redundancy circuit is configured to provide the read repair information for the read operation to any of the plurality of banks; and

wherein the second redundancy circuit is configured to provide the write repair information for the write operation to any of the plurality of banks.